

Totem-Pole Power Control for Processors
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The Claims:

1. (Original) A switched current power converter for an integrated circuit comprising

a capacitor for storing a charge to supply a voltage to the integrated circuit

a plurality of constant current sources

a plurality of switching means, there being one switching means for each of the plurality of constant current sources,

each of the plurality of switching means being connected respectively to one of the plurality of constant current sources,

each of the plurality of switching means being arranged and disposed so as to have a first switch state in which a current from a respective one of the plurality of constant current source is directed to the capacitor, and

each of the plurality of switching means being arranged and disposed so as to have a second switch state in which the current from the respective one of the plurality of constant current source is directed to return,

and at least one of the plurality of switching means is a totem pole cell located within the integrated circuit.

2. (Original) The switched current power converter of claim 1 further comprising at least one additional constant current source that is connected directly to the capacitor.

3. (Original) The switched current power converter of claim 1 wherein

at least one of the at least one of the plurality of switching means that is a totem pole cell located within the integrated circuit has a third switch state in which the totem pole cell is open, and

further comprising at least one outside switching means, located outside of the integrated circuit,

the at least one outside switching means being arranged and disposed so as to have a first switch state in which the current from the respective one of the plurality of constant current sources which is connected to the at least one of the at least one of the plurality of switching means that is a totem pole cell located within the integrated circuit is directed to return outside of the integrated circuit when the at least one of the at least one of the plurality of switching means that is a totem pole cell located within the integrated circuit is open, and

the at least one outside switching means has a second switching state in which the at least one outside switching means is open.

4. (Original) A data bus driver circuit having a data output comprising a first totem pole cell that is located within an integrated circuit,

the first totem pole cell comprising a first switching mean connected between the data output and a return,

the first totem pole cell comprising a second switching means connected between the data output and a power distribution circuit within the integrated circuit,

the data bus driver circuit further comprising a source of constant current located outside of the integrated circuit and connected to the data output,

the first totem pole cell has a first switch state in which the first switching means is closed and the second switching means is open so that the data output is essentially at a potential of the return and current from the source of constant current is directed to the return, and

the first totem pole cell has a second switch state in which the first switching means is open and the second switching means is closed so that the data output is essentially at the potential of the power distribution circuit within the integrated circuit and current from the source of constant current is directed to the power distribution circuit within the integrated circuit.

5. (Original) The data bus driver circuit of claim 4 wherein the first totem pole cell has a third switch state in which the first switching means and the second switching means are open,

and further comprising at least one additional totem pole cell located outside of the integrated circuit,

the at least one additional totem pole cell comprising a third switching means connected between the data output and the return,

the at least one additional totem pole cell comprising a fourth switching means connected between the data output and the power distribution circuit outside of the integrated circuit,

the at least one additional totem pole cell has a first switch state in which the third switching means is closed and the second switching means is open so that the data output is essentially at a potential of the return and current from the source of constant current is directed to the return, and

the at least one additional totem pole cell has a second switch state in which the third switching means is open and the fourth switching means is closed so that the data output is essentially at the potential of the power distribution circuit outside of the integrated circuit and current from the source of constant current is directed to the power distribution circuit outside of the integrated circuit.

6. (Currently amended) A ballast block for dividing a current from a source of constant current into a plurality smaller constant currents for driving a data bus comprising a plurality of totem pole data drivers each having a data output comprising a plurality of inductor means, one inductor means for each of the plurality of totem pole data drivers, an input end of each of the plurality of inductor means all being connected together in parallel and to the source of constant current and an output end of each of the plurality of inductor means each being connected to a respective data output of a respective one of the plurality of totem pole data drivers.

7. (Original) The ballast block of claim 6 wherein the ballast block comprises a block of ferrite having a plurality of through holes therein with wire conductors therein to comprise the plurality of inductor means.

8. (Original) The ballast block of claim 6 wherein the ballast block comprises a block of sintered powdered metal having a plurality of through holes therein with wire conductors therein to comprise the plurality of inductor means.

9. (Original) The ballast block of claim 6 wherein the ballast block comprises a parallel array of conductors, and the inductor means comprises the self inductance of the conductors of the parallel array of inductors.